

## CLAIMS

What is claimed is:

- 1        1.    An integrated circuit comprising:  
2                one or more functional blocks to perform one or  
3        more functions; and  
4                an on-chip frequency compensation circuit including  
5                        a selectively enabled reliability oscillator  
6                to generate a reference oscillating signal,  
7                        a clocked reliability oscillator to generate  
8                an AC degraded oscillating signal, and  
9                        a compare circuit coupled to the reliability  
10                oscillators, the compare circuit to compare the  
11                oscillating signals and to generate a frequency  
12                compensation signal in response to the comparison  
13                being greater than a predetermined threshold.
  
- 1        2.    The integrated circuit of claim 1, wherein  
2                the on-chip frequency compensation circuit further  
3        includes  
4                        a first counter coupled between the  
5                selectively enabled reliability oscillator and the  
6                compare circuit, the first counter to generate a  
7                reference count;

8                   a second counter coupled between the clocked  
9                   reliability oscillator and the compare circuit, the  
10                  second counter to generate a dynamic count; and  
11                  the compare circuit to compare the reference  
12                  count with the dynamic count.

1       3.    The integrated circuit of claim 2, wherein  
2            the on-chip frequency compensation circuit further  
3            includes

4                   a first prescaler coupled between the  
5                   selectively enabled reliability oscillator and the  
6                   first counter, the first prescaler to divide by N  
7                   the number of oscillations in an oscillating signal  
8                   from the selectively enabled reliability  
9                   oscillator; and

10                  a second prescaler coupled between the dynamic  
11                  reliability oscillator and the second counter, the  
12                  second prescaler to divide by N the number of  
13                  oscillations in an oscillating signal from the  
14                  dynamic reliability oscillator.

1       4.    The integrated circuit of claim 1, wherein  
2            the on-chip frequency compensation circuit further  
3            includes

4                   a static reliability oscillator to generate a  
5                   DC bias degraded oscillating signal.

1        5.    The integrated circuit of claim 4, wherein  
2            the on-chip frequency compensation circuit further  
3 includes  
4            a first counter coupled between the  
5            selectively enabled reliability oscillator and the  
6            compare circuit, the first counter to generate a  
7            reference count;  
8            a second counter coupled between the clocked  
9            reliability oscillator and the compare circuit, the  
10          second counter to generate a dynamic count;  
11          a third counter coupled between the static  
12          reliability oscillator and the compare circuit, the  
13          third counter to generate a static count; and  
14          the compare circuit to compare the reference  
15          count with the dynamic count and the reference  
16          count with the static count.

1        6.    The integrated circuit of claim 5, wherein  
2            the on-chip frequency compensation circuit further  
3 includes  
4            a first prescaler coupled between the  
5            selectively enabled reliability oscillator and the  
6            first counter, the first prescaler to divide by N  
7            the number of oscillations in an oscillating signal  
8            from the selectively enabled reliability  
9            oscillator;

10                   a second prescaler coupled between the dynamic  
11                   reliability oscillator and the second counter, the  
12                   second prescaler to divide by N the number of  
13                   oscillations in an oscillating signal from the  
14                   dynamic reliability oscillator; and

15                   a third prescaler coupled between the static  
16                   reliability oscillator and the third counter, the  
17                   third prescaler to divide by N the number of  
18                   oscillations in an oscillating signal from the  
19                   static reliability oscillator.

1           7.    The integrated circuit of claim 1, wherein  
2                the integrated circuit is a microprocessor.

1           8.    An integrated circuit comprising:  
2                one or more functional blocks; and  
3                an on-chip frequency compensation circuit including  
4                   a selectively enabled reliability oscillator  
5                to generate a reference oscillating signal,  
6                   a static reliability oscillator to generate a  
7                DC bias degraded oscillating signal, and  
8                   a compare circuit coupled to the reliability  
9                oscillators, the compare circuit to compare the  
10               oscillating signals and to generate a frequency  
11               compensation signal in response to the comparison  
12               being greater than a predetermined threshold.

1        9.    The integrated circuit of claim 8, wherein  
2            the on-chip frequency compensation circuit further  
3 includes

4            a first counter coupled between the  
5            selectively enabled reliability oscillator and the  
6            compare circuit, the first counter to generate a  
7            reference count;

8            a second counter coupled between the static  
9            reliability oscillator and the compare circuit, the  
10          second counter to generate a static count; and

11          the compare circuit to compare the reference  
12          count with the static count.

1        10. The integrated circuit of claim 9, wherein  
2            the on-chip frequency compensation circuit further  
3 includes

4            a first prescaler coupled between the  
5            selectively enabled reliability oscillator and the  
6            first counter, the first prescaler to divide by N  
7            the number of oscillations in an oscillating signal  
8            from the selectively enabled reliability  
9            oscillator; and

10          a second prescaler coupled between the dynamic  
11          reliability oscillator and the second counter, the  
12          second prescaler to divide by N the number of

13           oscillations in an oscillating signal from the  
14           static reliability oscillator.

1       11. The integrated circuit of claim 8, wherein  
2       the integrated circuit is a microprocessor.

1       12. An integrated circuit comprising:  
2       one or more functional blocks to perform one or  
3       more functions; and  
4       an on-chip frequency compensation circuit including  
5           a first reliability oscillator including a  
6       selectively powered on ring oscillator to avoid  
7       transistor degradation, the first reliability  
8       oscillator to generate a reference oscillating  
9       signal on a first oscillation output,  
10       a second reliability oscillator including a  
11       constantly powered ring oscillator to experience  
12       transistor degradation, the second reliability  
13       oscillator to generate a degraded oscillating  
14       signal on a second oscillation output,  
15       a first counter having an input to couple to  
16       the first oscillation output, the first counter to  
17       generate a reference count on a first count output,  
18       and  
19       a second counter having an input to couple to  
20       the second oscillation output, the second counter

21           to generate a degraded count on a second count  
22           output.

1       13. The integrated circuit of claim 12, wherein  
2           the on-chip frequency compensation circuit further  
3       includes

4               a first prescaler coupled between the first  
5           reliability oscillator and the first counter, the  
6           first prescaler to divide by N the number of  
7           oscillations in the reference oscillating signal;  
8       and

9               a second prescaler coupled between the second  
10          reliability oscillator and the second counter, the  
11          second prescaler to divide by N the number of  
12          oscillations in the degraded oscillating signal.

1       14. The integrated circuit of claim 12, wherein  
2           the second reliability oscillator includes a  
3           constantly powered static ring oscillator to  
4           experience DC static transistor degradation, the  
5           degraded oscillating signal is an DC bias degraded  
6           oscillating signal on the second oscillation  
7           output, and the degraded count is a static count.

1       15. The integrated circuit of claim 12, wherein  
2           the second reliability oscillator includes a  
3           constantly powered clocked ring oscillator to

4           experience AC dynamic transistor degradation, the  
5           degraded oscillating signal is an AC degraded  
6           oscillating signal on the second oscillation  
7           output, and the degraded count is a dynamic count.

1       16. The integrated circuit of claim 15, wherein  
2           the on-chip frequency compensation circuit further  
3       includes

4           a third reliability oscillator including a  
5           constantly powered static ring oscillator to  
6           experience DC static transistor degradation, the  
7           third reliability oscillator to generate a DC bias  
8           degraded oscillating signal on a third oscillation  
9           output, and

10          a third counter having an input to couple to  
11          the third oscillation output, the third counter to  
12          generate a static count on a third count output.

1       17. The integrated circuit of claim 16, wherein  
2           the on-chip frequency compensation circuit further  
3       includes

4           a first prescaler coupled between the first  
5           reliability oscillator and the first counter, the  
6           first prescaler to divide by N the number of  
7           oscillations in the reference oscillating signal,

8           a second prescaler coupled between the second  
9           reliability oscillator and the second counter, the



10           second prescaler to divide by N the number of  
11           oscillations in the dynamic oscillating signal, and  
12           a third prescaler coupled between the third  
13           reliability oscillator and the third counter, the  
14           third prescaler to divide by N the number of  
15           oscillations in the static oscillating signal.

1       18. The integrated circuit of claim 13, wherein  
2           the on-chip frequency compensation circuit further  
3       includes  
4           a state machine to start and stop the counting  
5       by the counters.

1       19. The integrated circuit of claim 13, wherein  
2           the first counter includes a count overflow output  
3       and a count enable input, the count overflow output  
4       being a stop signal is coupled to the count enable input  
5       to stop the first counter from counting further, and  
6           the on-chip frequency compensation circuit further  
7       includes  
8           a first synchronizer having an input coupled  
9           to the count overflow output and an output coupled  
10          to a count enable input of the second counter, the  
11          first synchronizer to synchronize the stop signal  
12          to stop the second counter from counting further.

1       20. The integrated circuit of claim 16, wherein

2           the first counter includes a count overflow output  
3           and a count enable input, the count overflow output  
4           being a stop signal is coupled to the count enable input  
5           to stop the first counter from counting further, and  
6           the on-chip frequency compensation circuit further  
7           includes  
8           a first synchronizer having an input coupled  
9           to the count overflow output and an output coupled  
10          to a count enable input of the second counter, the  
11          first synchronizer to synchronize the stop signal  
12          to stop the second counter from counting further,  
13          and  
14          a second synchronizer having an input coupled  
15          to the count overflow output and an output coupled  
16          to a count enable input of the third counter, the  
17          second synchronizer to synchronize the stop signal  
18          to stop the third counter from counting further.

1        21. The integrated circuit of claim 12, wherein  
2           a clock signal is coupled into a clock input of the  
3           second reliability oscillator.

1        22. The integrated circuit of claim 12, wherein  
2           the integrated circuit is a microprocessor.

1        23. A method in an integrated circuit with functional  
2           blocks, the method comprising:

3           enabling measurement of ring oscillator frequencies  
4   of a trio of ring oscillators;  
5           measuring a first frequency of a first ring  
6   oscillator having non-stressed transistors;  
7           measuring a second frequency of a second ring  
8   oscillator having stressed transistors;  
9           comparing the first frequency with the second  
10   frequency to determine a first measure of transistor  
11   degradation.

1       24.   The method of claim 23, wherein  
2           the stressed transistors of the second ring  
3   oscillator are dynamically stressed transistors.

1       25.   The method of claim 23, wherein  
2           the stressed transistors of the second ring  
3   oscillator are statically stressed transistors.

1       26.   The method of claim 25, further comprising  
2           measuring a third frequency of a third ring  
3   oscillator having dynamically stressed transistors; and  
4           comparing the first frequency with the third  
5   frequency to determine a second measure of transistor  
6   degradation.

1       27.   The method of claim 23 further comprising:

2 performing one or more functions with the  
3 functional blocks.

1 28. The method of claim 27, wherein  
2 the functional blocks include an execution unit to  
3 execute instructions; and  
4 the integrated circuit is a microprocessor.

1 29. The method of claim 23, wherein  
2 the first ring oscillator and the second ring  
3 oscillator have substantially similar circuits.

1 30. The method of claim 29, wherein  
2 the the second ring oscillator has degraded  
3 transistors; and  
4 the first ring oscillator has transistors without  
5 degradation.

1 31. The method of claim 23, wherein  
2 the comparing determines a new clock ratio,  
3 and if the new clock ratio is less than an initial  
4 clock ratio multiplied by a guard band, then the new  
5 clock ratio is output to a clock generator.

1 32. The method of claim 31, further comprising  
2 generating a clock signal using the new clock  
3 ratio.

1        33. A microprocessor integrated circuit comprising:  
2            an execution unit to execute instructions; and  
3            an integrated on-chip frequency compensation  
4 circuit including

5            a reference reliability oscillator to  
6 selectively generate a reference oscillating  
7 signal,

8            a degrading reliability oscillator to  
9 selectively generate a degraded oscillating signal,  
10 and

11           a measurement and comparison circuit coupled  
12 to the reliability oscillators, the measurement and  
13 comparison circuit to receive the reference  
14 oscillating signal and the degrading oscillating  
15 signal to generate a first measure of transistor  
16 degradation, the measurement and comparison circuit  
17 to receive the reference oscillating signal and the  
18 DC degraded oscillating signal to generate a second  
19 measure of transistor degradation.

1        34. The microprocessor integrated circuit of claim 33,  
2 wherein

3            the degrading reliability oscillator is a dynamic  
4 reliability oscillator that selectively generates an AC  
5 degraded oscillating signal.

1        35. The microprocessor integrated circuit of claim 33,  
2        wherein  
3            the degrading reliability oscillator is a static  
4        reliability oscillator that selectively generates a DC  
5        degraded oscillating signal.

1        36. The microprocessor integrated circuit of claim 35,  
2        further comprising  
3            a dynamic reliability oscillator to selectively  
4        generate an AC degraded oscillating signal, and  
5            the measurement and comparison circuit to receive  
6        the reference oscillating signal and the AC degraded  
7        oscillating signal to generate a first measure of  
8        transistor degradation, the measurement and comparison  
9        circuit to receive the reference oscillating signal and  
10       the DC degraded oscillating signal to generate a second  
11       measure of transistor degradation.

1        37. The microprocessor integrated circuit of claim 36,  
2        wherein  
3            the measurement and compare circuit further to  
4        compare the first measure of transistor degradation with  
5        the second measure of transistor degradation to  
6        determine a worst transistor degradation.

1        38. The microprocessor integrated circuit of claim 37,  
2        wherein  
3            the measurement and compare circuit to generate a  
4        frequency compensation signal in response to the worst  
5        transistor degradation being greater than a  
6        predetermined level.

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